

Henry Cheng

Serial No.: 09/643,981

Response to Office Action dated October 5, 2004

Amendments to the Specification:

Please replace the paragraph beginning at page 1, (numbered) line 5 with the following amended paragraph:

This application is related to application serial number 09/643,984, now U.S. Patent No. 6,643,744 [[_____]], entitled "Method and Apparatus for Pre-Fetching Audio Data" (~~att. dkt. no. 723-846~~), the contents of which are hereby incorporated by reference.

Please replace the paragraph beginning on page 7, line 20 with the following amended paragraph:

In this example, main processor 110 (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers 52 (and/or other input devices) via graphics and audio processor 114. Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied, for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive. As one example, in the context of video game play, main processor 110 can perform collision detection and animation processing in addition to a variety of interactive and control functions. Main memory 112 may, for example, comprise an SRAM, such as a 1T1SRAM, manufactured by Mosys ~~Moses~~ Corporation, which automatically performs internal refresh operations.

Please replace the paragraph beginning at page 15, line 14 with the following amended paragraph:

DSP core 811 has a 100 MHz instruction clock and uses 16-bit data words and addressing. DSP core 811 uses a word (16-bit) addressable instruction memory 813 that includes a RAM area (e.g., 8 kbyte) and a ROM area (e.g., 8 kbyte) and a word addressable data memory 815 that includes a RAM area (e.g., 8 kbyte) and a ROM area (e.g., 4 kbyte). A DSP DMA 819 is provided to transfer data from/to main memory 112 to/from the DSP data/instruction RAM areas or from the DSP data/instruction ROM areas to main memory 112. There are two requestors of access to instruction memory 813:

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DSP DMA 819 and DSP 811. The instruction RAM area can be read/write by DSP DMA 819 and can only be read by DSP 811. The instruction ROM area can only be read by DSP 811. There are three requestors of access to data memory 815: DSP DMA 819, data bus 1 and data bus 2. Mail box registers 817 are provided for communication with the main processor 110. Mail box registers 817 may include a first mail box register for communications from main processor 110 to DSP core 811 and a second mail box register for communications from DSP core 811 to main processor 110. Each register is, for example, 32-bits wide. An accelerator 821 is usable instead of DSP core 811 to read from and write to audio memory 126. A memory controller 823 is provided for audio memory 126 and is operative, among other things, to arbitrate requests for audio memory access between DSP core 811 and a dedicated DMA channel 825 controlled by main processor 110 for data transactions between audio memory 126 and main memory 112. Generally, data transactions between audio memory 126 and DSP data memory 815 have priority over DMA channel 825. Additional details of the audio system including details of memory controller 823 and DMA channel 825 may be found in Application No. 09/643,984, now U.S. Patent No. 6,643,744 [_____] (~~att. dkt. no. 723-846~~) entitled "Method and Apparatus for Pre-Fetching Data in Audio Memory", the contents of which are incorporated herein. A decoder 827 decodes audio samples supplied thereto. Audio memory 126 is intended primarily for the storage of audio-related data and may comprise 16 MB of SDRAM (expandable up to a total of 48 MB).

Please replace the paragraph beginning at page 26, line 4 with the following amended paragraph:

The mixer and effects processor described ~~above~~ below separately provide effects for signals on three or more channels such as left, right and surround channels. Therefore, effects may be selectively "positioned" in three-dimensional space to provide enhanced audio content. The mixer is symmetrical in that the number of effects (auxiliary) sends/returns is the same as the number of mixing/accumulating channels. While the example mixer described above uses three mixing/accumulating channels and three sends/returns, the scope of the invention is not limited in this respect and is readily

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applicable, for example, to systems having more than three mixing/accumulating channels. Thus, the invention is applicable to any system having channels for three or more of a left channel, a right channel, a surround channel, a left surround channel, a right surround channel, a center channel, a low-frequency effects channel, and the like. Thus, the teachings of the present application are readily applied to systems such as AC3 that utilize six mixing/accumulating channels and would therefore involve six effects (auxiliary) sends/returns.